

Multilayer Ceramic Chip Capacitors

Introduction

Multilayer Surface Mount Ceramic Capacitors are constructed by screen printing alternative layers of internal metallic electrodes onto ceramic dielectric materials and firing into a concrete monolithic body, then completed by application of metal end terminations which are fired to assure permanent bonding with the individual internal electrodes.

Multilayer ceramic capacitors have various features such as large capacitance values in small sizes and excellent high frequency characteristics.

Moreover, chip capacitors can be used on surface mount assembly equipment. Our fully integrated manufacturing and total quality control systems ensure unprecedented high standards of quality and reliability.

Chip Capacitor Selection

Selection of the most suitable capacitor for any application is based on the following:

Dielectric Type

The choice of dielectric is largely determined by the temperature stability required.

COG (NPO)

Capacitance change with temperature is 0-30ppm/°C which is less than -0.3%/°C from -55°C to +125°C. Typical capacitance change with life is less than -0.1% for NPOs, one-fifth that shown by most other dielectrics. NPO formulations show no aging characteristics.

X7R

Its temperature variation of capacitance is within $\pm 15\%$ from -55°C to +125°C. This capacitance change is non-linear.

Z5U

Despite their capacitance instability, Z5U formulations are very popular because of their small size, low ESL, low ESR and excellent frequency response. These features are particularly important for decoupling application where only a minimum capacitance value is required.

Y5V

Y5V formulations are for general purpose use in a limited temperature range. They have a wide temperature characteristic of +22% - 82% capacitance change over the operating temperature range of -30°C to +85°C. Y5Vs high dielectric constant allows the manufacture of very high capacitance value (up to 22MF) in small physical sizes.

Capacitance Value & Tolerance

Determined by circuit requirements. Note that chip prices decrease with lower capacitance value and looser tolerance.

Voltage

Determined by circuit requirements. Units are designed to exceed the withstanding voltage specification, i.e., the user need not incorporate an additional safety margin.

Capacitor Size

Select the smallest unit permitted by the circuit constraints that provides the required capacitance and voltage rating. Smaller units are generally less expensive : 0805 is the most economical size.

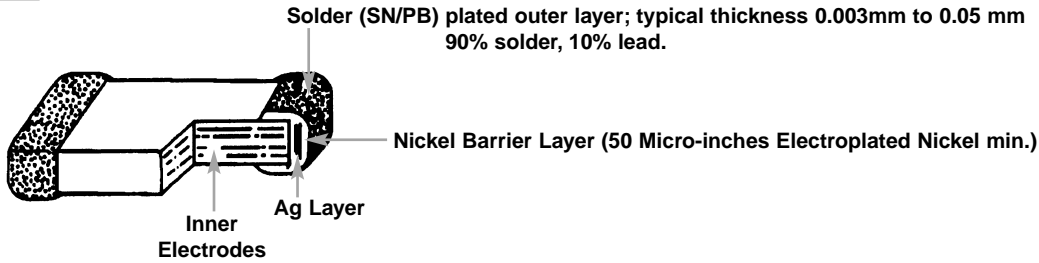
Capacitor Termination

Termination choice is largely determined by the chip attachment method. Silver-palladium is adequate for most applications involving soldering or solder reflow.

Nickel barrier is standard and recommended for units exposed to repeated solder cycles, to minimize leaching of the termination.

Multilayer Ceramic Chip Capacitors

Construction

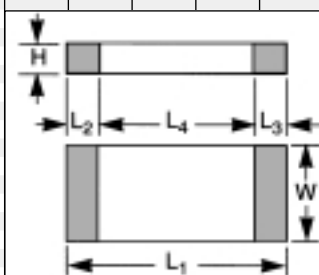


Example

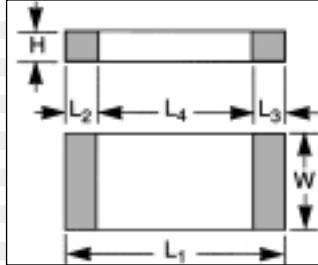
GMC21	CG	102	J	50	N	T	M																																																					
Size Code	Dielectric	Capacitance (pF)	Capacitance Tolerance (EIA Code)	Voltage	Termination	Packaging Code	Designates EIA Marked Parts																																																					
	CG (COG)(NPO) X7R Z5U Y5V																																																											
<p>Capacitance values are represented in 3 digits, and expressed in pF. The first two digits are significant, and the third is the number of zeros. The letter "R" is used as a decimal point.</p> <table border="1"> <tr><td>0R5</td><td>0.5pF</td></tr> <tr><td>5R0</td><td>5pF</td></tr> <tr><td>100</td><td>10pF</td></tr> <tr><td>101</td><td>100pF</td></tr> </table>		0R5	0.5pF	5R0	5pF	100	10pF	101	100pF	<table border="1"> <tr><td>B</td><td>±0.1pF</td><td>for ≤10pF</td></tr> <tr><td>C</td><td>±0.25pF</td><td>for ≤10pF</td></tr> <tr><td>D</td><td>±0.5pF</td><td>for ≤10pF</td></tr> <tr><td>F</td><td>±1%</td><td>for ≤10pF</td></tr> <tr><td>G</td><td>±2%</td><td></td></tr> <tr><td>H</td><td>±3%</td><td></td></tr> <tr><td>J</td><td>±5%</td><td></td></tr> <tr><td>K</td><td>±10%</td><td></td></tr> <tr><td>M</td><td>±20%</td><td></td></tr> <tr><td>Z</td><td>-20%~+80%</td><td></td></tr> </table>	B	±0.1pF	for ≤10pF	C	±0.25pF	for ≤10pF	D	±0.5pF	for ≤10pF	F	±1%	for ≤10pF	G	±2%		H	±3%		J	±5%		K	±10%		M	±20%		Z	-20%~+80%		<table border="1"> <tr><td>16</td><td>16 DC</td></tr> <tr><td>25</td><td>25 DC</td></tr> <tr><td>50</td><td>50 DC</td></tr> <tr><td>100</td><td>100 DC</td></tr> <tr><td>200</td><td>200 DC</td></tr> </table>	16	16 DC	25	25 DC	50	50 DC	100	100 DC	200	200 DC	<table border="1"> <tr><td>N</td><td>Nickel Barrier</td></tr> <tr><td>T</td><td>Card Board Taping</td></tr> <tr><td>E</td><td>Embossed Taping</td></tr> </table>	N	Nickel Barrier	T	Card Board Taping	E	Embossed Taping	<table border="1"> <tr><td>0805 to 2225</td></tr> </table>	0805 to 2225
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***NOTE:** Cal-Chip is phasing out marked capacitors as it is not cost effective. Our engineers also believe it weakens the durability of the component over its life due to the laser etching marking technique used.

		GMC04						GMC10											
Type		0402						0603											
Length (L ₁)	mm	1.0±0.05						1.6±0.2											
	inches	0.04±0.002						0.063±0.008											
Width (W)	mm	0.5±0.05						0.8±0.2											
	inches	0.02±0.002						0.031±0.008											
Thickness (H)	mm	0.5±0.1						0.8±0.2											
	inches	0.02±0.004						0.031±0.008											
Termination Band (L ₂ & L ₃)	mm	Min 0.1			Max 0.35			Min 0.1			Max 0.4								
	inches	0.004			0.014			0.004			0.015								
Band Gap (L ₄) (Min)	mm	0.3						0.6											
	inches	0.012						0.015											
Dielectric		COG		X7R		Y5V		COG		X7R		Y5V							
Rated Voltage d.c.		25	50	16	25	50	25	50	25	50	100	10	16	25	50	16	25	50	
Cap. Range	Code	Minimum and Maximum capacitance values available																	
0.5pF	0p5																		
1.0	1p0																		
1.2	1p2																		
1.5	1p5																		
1.8	1p8																		
2.2	2p2																		
2.7	2p7																		
3.3	3p3																		
3.9	3p9																		
4.7	4p7																		
5.6	5p6																		
6.8	6p8																		
8.2	8p2																		
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470	474																		
560	564																		
680	684																		
820	824																		
1.0µF	105																		



CCE Part Number		GMC21	GMC29	GMC31	GMC32	GMC43	GMC45	GMC55	GMC57
Type		0805	0907	1206	1210	1812	1825	2220	2225
Dimensions									
Length (L ₁)	mm	2.0±0.03	2.3±0.3	3.2±0.3	3.2±0.3	4.5±0.35	4.5±0.35	5.7±0.4	5.7±0.4
	inches	0.08±0.012	0.09±0.012	0.125±0.012	0.125±0.012	0.18±0.014	0.18±0.014	0.225±0.016	0.225±0.016
Width (W)	mm	1.25±0.02	1.8±0.3	1.6±0.2	2.5±0.3	3.2±0.3	6.3±0.4	5.0±0.4	6.3±0.4
	inches	0.05±0.008	0.071±0.012	0.063±0.008	0.10±0.012	0.125±0.012	0.25±0.016	0.197±0.016	0.25±0.016
Thickness (H)	mm	1.3	1.3	1.6	1.8	1.8	1.8	1.8	1.8
	inches	0.051	0.051	0.063	0.07	0.07	0.07	0.07	0.07
Termination Band (L ₂ & L ₃)	mm	Min 0.25 Max 0.75	Min 0.25 Max 0.75	Min 0.25 Max 0.75	Min 0.25 Max 0.75	Min 0.25 Max 0.75	Min 0.25 Max 0.75	Min 0.25 Max 0.75	Min 0.25 Max 0.75
	inches	0.01 0.03	0.01 0.03	0.01 0.03	0.01 0.03	0.01 0.03	0.01 0.03	0.01 0.03	0.01 0.03
Band Gap (L ₄) (Min)	mm	0.5	0.5	1.4	1.4	2.2	2.2	2.9	2.9
	inches	0.019	0.019	0.055	0.055	0.087	0.087	0.114	0.114
Related Voltage d.c.		50/63 100 200	50/63 100 200	50/63 100 200	50/63 100 200	50/63 100 200	50/63 100 200	50/63 100 200	50/63 100 200
Cap. Range	Code	Minimum and Maximum capacitance values available							
0.5pF	0p5								
1.0	1p0								
1.2	1p2								
1.5	1p5								
1.8	1p8								
2.2	2p2								
2.7	2p7								
3.3	3p3								
3.9	3p9								
4.7	4p7								
5.6	5p6								
6.8	6p8								
8.2	8p2								
10	100								
12	120								
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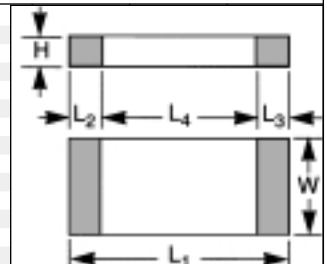


- Notes:**
1. Capacitance values to the E24 range also available.
 2. Higher capacitance values may be available with a corresponding increase in thickness.
 3. Sizes 1005 and 1808 are available as a special requirement.
 4. Chips to a specified thickness can be supplied as a special requirement.

Multilayer Ceramic Chip Capacitors - Size & Capacitance Table - Ultra Stable Dielectric

16 & 25V

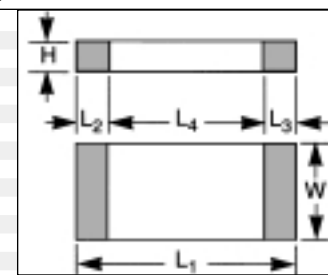
COG Dielectric		GMC21		GMC31		GMC32		GMC43		GMC55		GMC57	
Type		0805		1206		1210		1812		2220		2225	
Dimensions													
Length (L ₁)	mm	2.0±0.3		3.2±0.3		3.2±0.3		4.5±0.35		5.7±0.4		5.7±0.4	
	inches	0.08±0.012		0.125±0.012		0.125±0.012		0.18±0.014		0.225±0.016		0.225±0.016	
Width (W)	mm	1.25±0.2		1.6±0.2		2.5±0.3		3.2±0.3		5.0±0.4		6.3±0.4	
	inches	0.05±0.008		0.063±0.008		0.10±0.012		0.125±0.012		0.197±0.016		0.25±0.016	
Thickness (H)	mm	1.3		1.6		1.8		1.8		1.8		1.8	
	inches	0.051		0.063		0.07		0.07		0.07		0.07	
Termination Band (L ₂ &L ₃)	mm	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
	inches	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75
Band Gap (L ₄) (Min)	mm	0.5		1.4		1.4		2.2		2.9		2.9	
	inches	0.019		0.055		0.055		0.087		0.114		0.114	
Rated Voltage d.c.		16	25	16	25	16	25	16	25	16	25	16	25
Cap. Range	Code	Minimum and Maximum capacitance values available											
0.5pF	0p5												
1.0	1p0												
1.2	1p2												
1.5	1p5												
1.8	1p8												
2.2	2p2												
2.7	2p7												
3.3	3p3												
3.9	3p9												
4.7	4p7												
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100	104												



Multilayer Ceramic Chip Capacitors - Size & Capacitance Table - Stable Dielectric

10, 16 & 25V

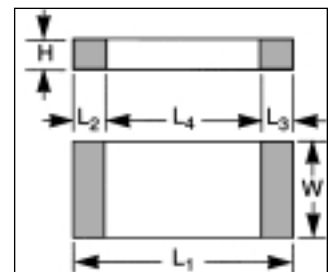
X7R Dielectric		GMC21			GMC31			GMC32		GMC43		GMC45		GMC55		GMC57	
Type		0805			1206			1210		1812		1825		2220		2225	
Dimensions		□			□			□		□		□		□		□	
Length (L ₁)	mm	2.0±0.3			3.2±0.3			3.2±0.3		4.5±0.35		4.5±0.35		5.7±0.4		5.7±0.4	
	inches	0.08±0.012			0.125±0.012			0.125±0.012		0.18±0.014		0.18±0.014		0.225±0.016		0.225±0.016	
Width (W)	mm	1.25±0.2			1.6±0.2			2.5±0.3		3.2±0.3		6.3±0.4		5.0±0.4		6.3±0.4	
	inches	0.05±0.008			0.063±0.008			0.10±0.012		0.125±0.012		0.025±0.016		0.197±0.016		0.25±0.016	
Thickness (H)	mm	1.3			1.6			1.8		1.8		1.8		1.8		1.8	
	inches	0.051			0.063			0.07		0.07		0.07		0.07		0.07	
Termination Band (L ₂ &L ₃)	mm	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
	inches	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75
		0.01	0.03	0.01	0.03	0.01	0.03	0.01	0.03	0.01	0.03	0.01	0.03	0.01	0.03	0.01	0.03
Band Gap (L ₄) (Min)	mm	0.5			1.4			1.4		2.2		2.2		2.9		2.9	
	inches	0.019			0.055			0.055		0.087		0.087		0.114		0.114	
Rated Voltage d.c		10	16	25	10	16	25	16	25	16	25	16	25	16	25	16	25
Cap. Range	Code	Minimum and Maximum capacitance values available															
100pF	101																
120	121																
150	151																
180	181																
220	221																
270	271																
330	331																
390	391																
470	471																
560	561																
680	681																
820	821																
1.0nF	102																
1.2	122																
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680	684																
820	824																
1.0µF	105																
1.2	125																
1.5	155																
1.8	185																
2.2	225																
2.7	275																
3.3	335																
3.9	395																
4.7	475																
5.6	565																
6.8	685																
8.2	825																
10	106																
15	156																
22	226																



Multilayer Ceramic Chip Capacitors - Size & Capacitance Table - General Purpose Dielectric

10, 16 & 25V

Z5U/Y5V Dielectric		GMC21		GMC31			GMC32		GMC43		GMC45		GMC55		GMC57		
Type		0805		1206			1210		1812		1825		2220		2225		
Dimensions		□		□			□		□		□		□		□		
Length (L ₁)	mm	2.0±0.3		3.2±0.3			3.2±0.3		4.5±0.35		4.5±0.35		5.7±0.4		5.7±0.4		
	inches	0.08±0.012		0.125±0.012			0.125±0.012		0.18±0.014		0.18±0.014		0.225±0.016		0.225±0.016		
Width (W)	mm	1.25±0.2		1.6±0.2			2.5±0.3		3.2±0.3		6.3±0.4		5.0±0.4		6.3±0.4		
	inches	0.05±0.008		0.063±0.008			0.10±0.012		0.125±0.012		0.25±0.016		0.197±0.016		0.25±0.016		
Thickness (H)	mm	1.3		1.6			1.8		1.8		1.8		1.8		1.8		
	inches	0.051		0.063			0.07		0.07		0.07		0.07		0.07		
Termination Band (L ₂ &L ₃)	mm	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
	inches	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75
Band Gap (L ₄) (Min)	mm	0.5		1.4			1.4		2.2		2.2		2.9		2.9		
	inches	0.019		0.055			0.055		0.087		0.087		0.114		0.114		
Rated Voltage d.c		16	25	10	16	25	16	25	16	25	16	25	16	25	16	25	
Cap. Range	Code	Minimum and Maximum capacitance values available															
1.0nF	102																
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68	683																
100	104																
150	154																
220	224																
330	334																
470	474																
680	684																
1.0µF	105																
1.5	155																
2.2	225																
3.3	335																
4.7	475																
6.8	685																
10	106																
15	156																
22	226																
27	276																
33	336																
39	396																
47	476																

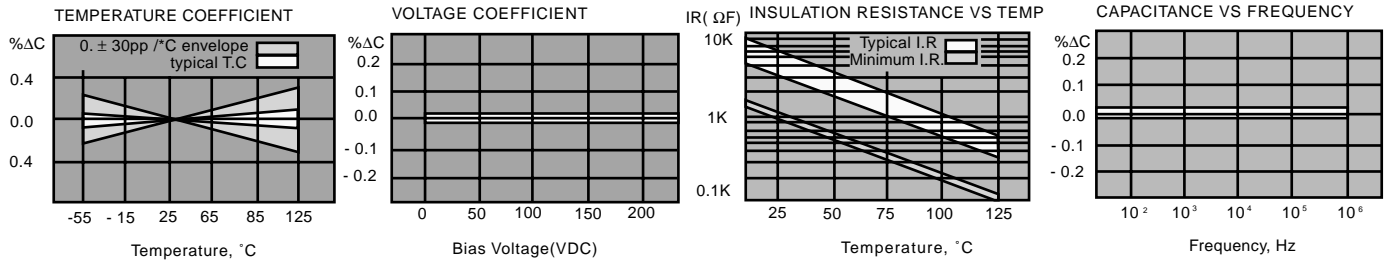


Multilayer Ceramic Chip Capacitors

COG Dielectric

Ultra stable class I dielectric: linear temperature coefficient, low loss, negligible change of electrical properties with time, voltage and frequency.

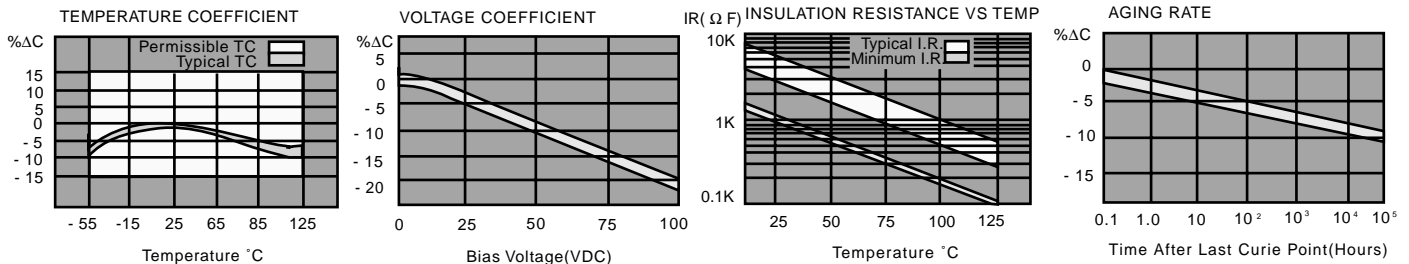
Operating Temperature Range	Temperature Coefficient	Temperature Voltage Coefficient (ΔC_{Max} @ V_{DCW})	Dissipation Factor	Insulation Resistance	Dielectric withstanding Voltage	Aging Rate	Test Parameters
-55°C to +125°C	0 \pm 30ppm/°C	0 \pm 30ppm/°C	0.1% Max, 0.02% Typical	<ul style="list-style-type: none"> •25°C, V_{DCW}:: >100GΩF or 1000ΩF, whichever is less •125°C, V_{DCW}:: >10GΩF or 100ΩF whichever is less 	2.5 X V_{DCW}	0% per decade hour	<ul style="list-style-type: none"> •C\leq51000pF f=1MHz V=1.0Vrms \pm0.2Vrms T=25°C •C>1000pF f=1KHz V=1.0Vrms \pm0.2Vrms T=25°C



X7R Dielectric

Stable class 11 dielectric (EIA X7R)

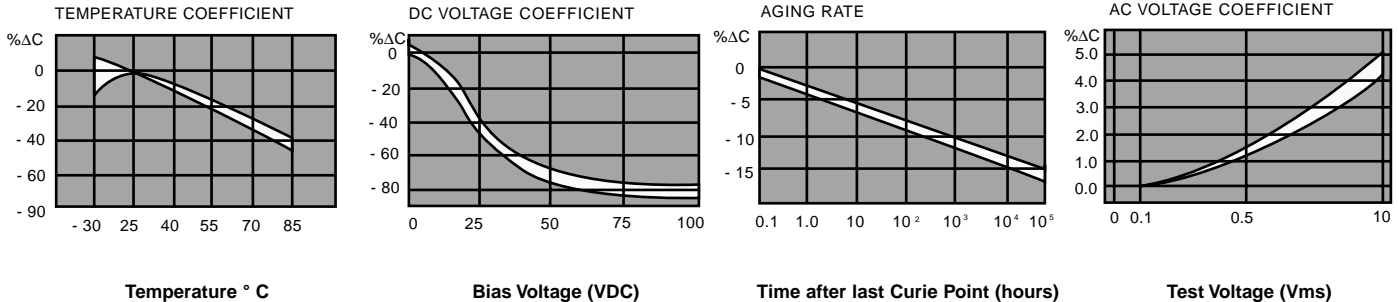
Operating Temperature Range	Temperature Coefficient	Temperature Voltage Coefficient (ΔC_{Max} @ V_{DCW})	Dissipation Factor	Insulation Resistance	Dielectric withstanding Voltage	Aging Rate	Test Parameters
55°C to +125°C	\pm 15%	X7R Not Applicable	2.5%Max, 1.8% Typical	<ul style="list-style-type: none"> •25°C, V_{DCW}:: >100GΩFor 1000ΩF, whichever is less •125°C, V_{DCW}:: >10GΩF or 100ΩF whichever is less 	2.5 X V_{DCW}	<2% per decade hour	1KHz, 1.0Vrms \pm 0.2Vrms 25°C



Multilayer Ceramic Chip Capacitors - Z5U (Y5V) Dielectric

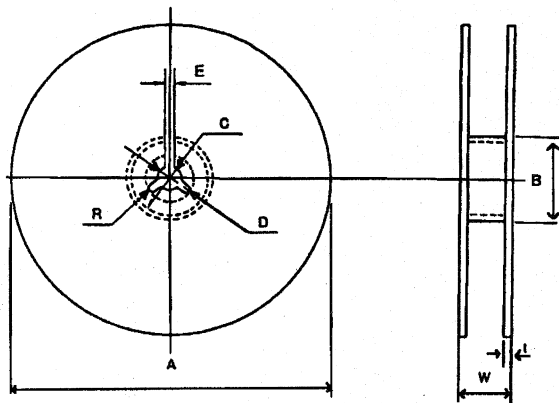
High capacitance per unit volume: general purpose product

Operating Temperature Range	Temperature Coefficient	Dissipation Factor	Insulation Resistance	Dielectric withstanding Voltage	Aging Rate	Test Parameters
-30°C to +85°C	+22% -82%	3.0% Max, 2.0% Typical	10GΩ or 100ΩF whichever is less, 25°C, V _{DCW}	2.5 X V _{DCW}	3.0% per decade hour	1KHz, 0.5 V _{rms} 25°C



Packaging (Taping)

(Reel Type-Size)



Standard Reel

Unit:mm

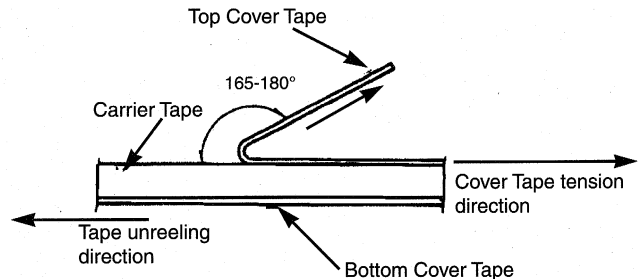
A	B	C	D	E	W	t	R
ø178 ±2.0	ø50 min.	ø13.0 ±0.5	ø21.0 ±0.8	2.0 ±0.5	14.9 ±1.5	0.8 ±0.2	1.0

10000 units per reel OPTIONAL

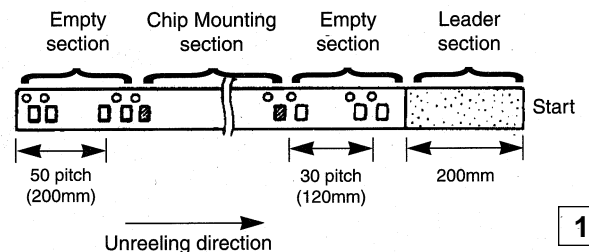
Unit:mm

A	B	C	D	E	W	t	R
ø250 ±2.0	ø50 min.	ø13.0 ±0.5	ø21.0 ±0.8	2.0 ±0.5	10.0 ±1.5	0.8 ±0.2	1.0

Carrier Tape (Standard)



- To peel off the cover tape by the method shown in the right figure apply a peel-off force of 20 gf - 60 gf (card board); 35 gf - 75 gf (plastic tape).
- The cover tape should not touch the top or bottom of the chip.
- If the cover tape has been peeled off it may be difficult to remove the chip due to punch-hole clearance, dirt, and debris. Make sure therefore that no paper waste will adhere to and block the absorption nozzle.
- If the cover tape has been peeled off from the top, stick it back on with a suitable adhesive.
- Follow the illustration for the start and end of the winding operation.



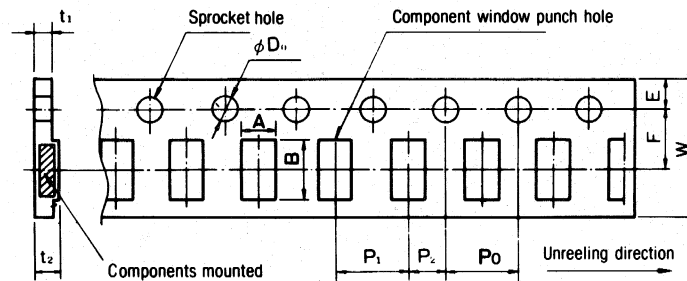
Multilayer Ceramic Chip Capacitors

• Cardboard carrier tape for 0402, 0603 type and 0805/1206 type

Unit: mm

Type	B	F	P1	P0	t1								Mounting Hole	Quantity per Reel
A	W	E	P2	D0	t2									
0402	0.7±0.2	1.3±0.2				2.0±0.05							Angular Punch Hole	10000
0603	1.1±0.2	1.9±0.2										4000		
0805	1.65±0.2	2.4±0.2	8.0±0.3	3.5±0.05	1.75±0.1	4.0±0.1	2.0±0.05	4.0±0.1	∅1.5 ^{+0.1} ₋₀	1.1 max	1.4 max	4000 to 5000*		
1206	2.0±0.2	3.6±0.2										4000 to 5000*		

*Dependent on chip thickness

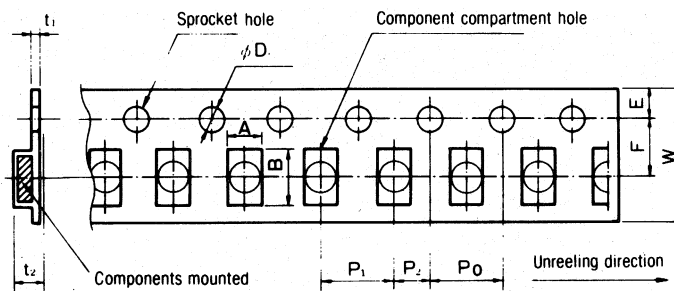


• Embossed plastic carrier tape for 0805/1206 type and 1210 type

Unit: mm

Type	A	B	W	F	E	P1	P2	P0	D0	t1	t2	Mounting Hole	Quantity per Reel
0805	1.45±0.2	2.3±0.2	8.0±0.3	3.5±0.05	1.75±0.1	4.0±0.1	2.0±0.05	4.0±0.1	∅1.5 ^{+0.1} ₋₀	0.6max	2.5 max	Angular	2000 to 5000*
1206	2.0±0.2	3.6±0.2										Embossed	2000 to 5000*
1210	2.9±0.2	3.6±0.2										Hole	2000 to 4000*

*Dependent on chip thickness

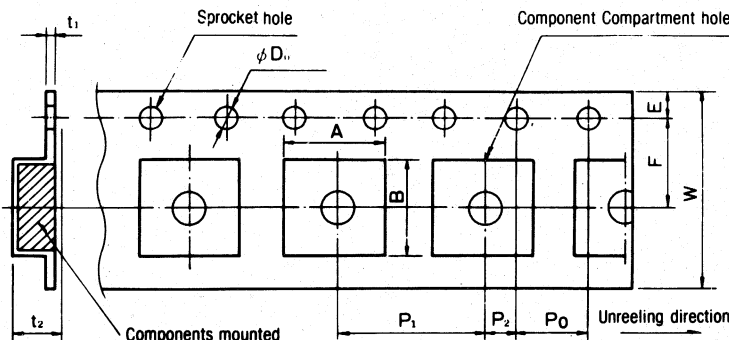


• Embossed plastic carrier tape for 1812, 1825, 2220 and 2225 type

Unit: mm

Type	A	B	W	F	E	P1	P2	P0	D0	t1	t2	Mounting Hole	Quantity per Reel
1812	3.6±0.2	4.9±0.2	12.0±0.3	5.5±0.05	1.75±0.1	8.0±0.1	2.0±0.05	4.0±0.1	∅1.5±0.1	0.6 max.	6.5 max.	Angular Embossed Hole	1000
1825	6.8±0.3	4.9±0.2											1000
2220	5.5±0.3	6.2±0.3											1000
2225	6.8±0.3	6.2±0.3											1000

*Dependent on chip thickness



Multilayer Ceramic Chip Capacitors - All Dielectrics

Tape and Reel Packing Quantities

Chip Size	178 mm (7") Reel	330 mm (13") Reel
0402	10,000	N/A
0603	4,000	16,000
0805	4,000	12,000
0907	3,000	12,000
1206	4,000	15,000
1210	2,000, 4,000	8,000
1812	1,000	4,000
1825	1,000	4,000
2220	1,000	4,000
2225	1,000	4,000

The tape and reel packing quantities apply to voltages up to 200V rating only.

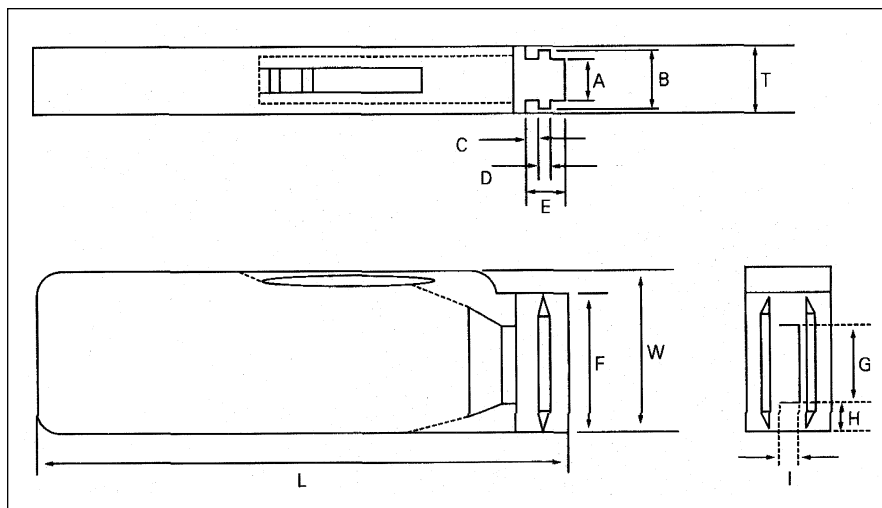
The 0402 and 0603 size chips have similar width and thickness dimensions.

Multilayer Ceramic Chip Capacitors

BULK CASE

- Bulk case packaging can reduce the stock space and transportation costs.
- The bulk feeding system can increase the productivity.
- It can eliminate the components loss.

- Structure and Dimension



Symbol	A	B	T	C	D	E
Dimension	6.8±0.1	8.8±0.1	12±0.1	1.5 ^{+0.1} , ₋₀	2 ⁺⁰ , _{-0.1}	4.7±0.1

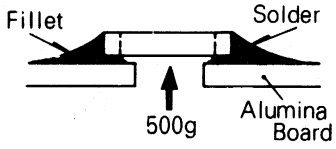
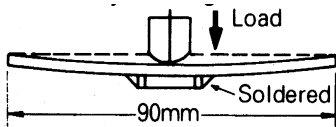
Symbol	F	W	G	H	L	I
Dimension	31.5 ^{+0.2} , ₋₀	36 ⁺⁰ , _{-0.2}	19±0.35	7±0.35	110±0.7	5±0.35

- Quantity

Size	04(0402)	10(0603)	21(0805)	
			T≤0.85mm	T≥1.0mm
Quantity	80,000	15,000	10,000	5,000

Multilayer Ceramic Chip Capacitors

RELIABILITY AND TEST CONDITIONS

Item	Specification	Test Method
Capacitance	Within tolerance shown by part number code	<ul style="list-style-type: none"> Class (1) C<1000pF:1MHz±10%, 0.5 to 5Vrms C≥1000pF:1KHz±10%, 1.0±0.2Vrms
Dissipation Factor (tanδ or Q)	<ul style="list-style-type: none"> Class (I) C<30pF:Q≥400+20xC C≥30pF:Q≥1000 Class (II) B:DF≤2.5% F:DF≤5.0% 	<ul style="list-style-type: none"> Class (II) 1KHz±10%, 1.0±0.2Vrms
Insulation Resistance(IR)	C≤10,000pF:IR≥100GΩ C>10,000pF:IR≥500/C	Apply rated voltage for 60 seconds at room temperature and normal humidity. (70% RH max)
Dielectric Withstanding Voltage	There shall be no evidence of damage or flash over during the test	Apply 3 x rated voltage (Class I) or 2.5 x rated voltage (Class II) to both terminations for 5 seconds. Charge and discharge current are less than 50mA.
Termination Adherence	No mechanical damage	 <p>Care shall be taken to avoid thermal shock. 500g of steady pull is applied in direction of arrow for 1 minute.</p>
Bend Strength	No mechanical damage	<p>After soldering capacitor on the glass-epoxy PWB, 2 mm of vending shall be applied for 10 seconds as shown by drawing.</p> 
Life Test (High Temperature Loading Test)	ΔC	Applied 2 x rated voltage at maximum operating temperature for 1000 hours. The surge current shall not exceed 50mA after above testing condition, test samples shall be kept in room temperature for 24 hours (Class I) or 48 hours (Class II), and then shall be measured.
	Q or DF	
	IR	

Multilayer Ceramic Chip Capacitors

RELIABILITY AND TEST
CONDITIONS

Item	Specification	Test Method
Moisture Test	ΔC <ul style="list-style-type: none"> Class (I) No more than $\pm 5\%$ or $\pm 0.5\text{pF}$ whichever is larger Class (II) B: $\pm 10\%$ F: $\pm 30\%$ 	<p>The capacitors shall be subjected to 40°C, 90-95%RH for 500 hours.</p> <p>After above testing condition, samples shall be kept in room temperature for 24 hours (Class I) or 48 hours (Class II), and then shall be measured.</p>
	Q or DF <ul style="list-style-type: none"> Class (I) $C < 10\text{pF}$: $Q > 200 + 10 \times C$ $10 \leq C < 30\text{pF}$: $Q \geq 275 + 5/2 \times C$ $C \geq 30\text{pF}$: $Q \geq 350$ Class (II) B: $DF \leq 5.0\%$ F: $DF \leq 7.5\%$ 	
	IR 1000M Ω or 50 ΩF , whichever is less	
Moisture Resistance Test	ΔC <ul style="list-style-type: none"> Class (I) No more than $\pm 7.5\%$ or $\pm 0.75\text{pF}$ whichever is larger Class (II) B: $\pm 10\%$ F: $\pm 30\%$ 	<p>Apply rated voltage at 40°C, 90-95%RH for 500 hours.</p> <p>The surge current shall not exceed 50mA. After testing with above condition, samples shall be kept in room temperature for 24 hours (Class I) or 48 hours (Class II), and then shall be measured.</p>
	Q or DF <ul style="list-style-type: none"> Class (I) $C < 30\text{pF}$: $Q > 100 + 100/3 \times C$ $C \geq 30\text{pF}$: $Q \geq 200$ Class (II) B: $DF \leq 5.0\%$ F: $DF \leq 7.5\%$ 	
	IR 500M Ω or 25 ΩF , min whichever is less	
Temperature Cycle	ΔC <ul style="list-style-type: none"> Class (I) No more than $\pm 2.5\%$ or $\pm 0.25\text{pF}$ whichever is larger Class (II) B: $\pm 5\%$ F: $\pm 20\%$ 	<p>Perform 5 cycles as follow:</p> <ol style="list-style-type: none"> Room temperature. Dwell for 15 minutes. Minimum operating temperature, dwell for 30 minutes. Room temperature, dwell for 30 minutes. Maximum operating temperature, dwell for 30 minutes. <p>After above testing condition, samples shall be kept in room temperature for 24 hours (Class I) or 48 hours (Class II), and then shall be measured.</p>
	Q or DF To satisfy the specified initial value.	
	IR To satisfy the specified initial value.	
Solderability	Termination area shall be at least 95% covered with a new solder coating. There shall be no crack and ceramic exposure of terminated surface by melting.	The capacitors are completely immersed during 4 ± 0.5 seconds in the molten solder with a temperature of $230 \pm 5^\circ\text{C}$ *Solder: Sn 63.
Resistance to Solder Heat Test	ΔC <ul style="list-style-type: none"> Class (I) No more than $\pm 2.5\%$ or $\pm 0.25\text{pF}$ whichever is larger Class (II) B: $\pm 5\%$ F: $\pm 20\%$ 	<p>Immerse into molten solder at $270 \pm 5^\circ\text{C}$ for 3 ± 0.5 seconds. Preheat before immersion.</p> <ol style="list-style-type: none"> $80\text{--}100^\circ\text{C}$ for 2 minutes. $150\text{--}180^\circ\text{C}$ for 2 minutes. $270 \pm 5^\circ\text{C}$ for 3 ± 0.5 seconds. <p>The capacitance, measurement shall be made after sample keeping at room temperature for 24 hours.</p>
	Q or DF To satisfy the specified initial value.	
	IR To satisfy the specified initial value.	

Multilayer Ceramic Chip Capacitors

APPLICATION MANUAL FOR
SURFACE MOUNTING

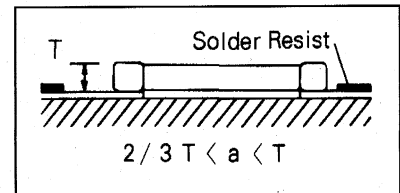
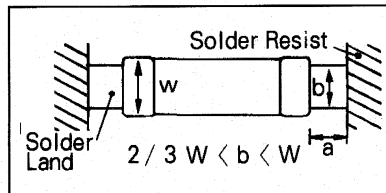
1. Temperature / Humidity Control

Since dew condensation may occur by the differences in temperature when the products are take out of storage, it is important to maintain a temperature-controlled environment.

2. Design of Solder Land Pattern

When designing printed circuit boards, the shape and size of the solder lands must allow for the proper amount of solder on the capacitor. The amount of solder at the end terminations has a direct effect on the probability that the chip will crack. The greater amount of solder, the larger amount of stress on the chip, and the more likely that it will break. Use the following illustrations as guidelines for proper solder land design.

Recommendation of solder land shape and size.



3. Adhesives

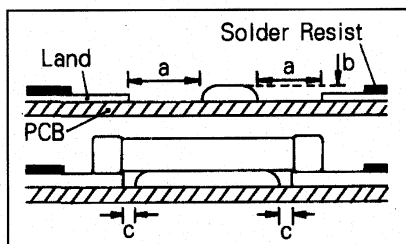
MLCCs generally require the use of an adhesive to adhere the chips to the circuit board prior to wave soldering.

3-1. Requirements for Adhesives

- They must have enough adhesion so that the chips will not fall off or move during the handling of the circuit board.
- They must maintain their adhesive strength when exposed to soldering temperatures.
- They should not spread or run when applied to the circuit board.
- They should have a long pot life.
- They should harden quickly.
- They should not corrode the circuit board or chip material.
- They should be a good insulator.
- They should be non-toxic, and not produce harmful gases, nor be harmful when touched.

3-2. Application Method

It is important to use the proper amount of adhesive. Too little will cause poor adhesion to the circuit board, and too much may strain the conductor pattern, thereby causing defective soldering. The following illustrations show the proper quantity of adhesive.



(Unit: mm)

Type	21	31
a	0.2 min	0.2 min
b	70~100μm	70~100μm
c	>0	>0

3-3. Adhesive Hardening Characteristics

To prevent oxidation of the terminations, the adhesive must harden at 160°C or less, within 2 minutes or less.

Multilayer Ceramic Chip Capacitors

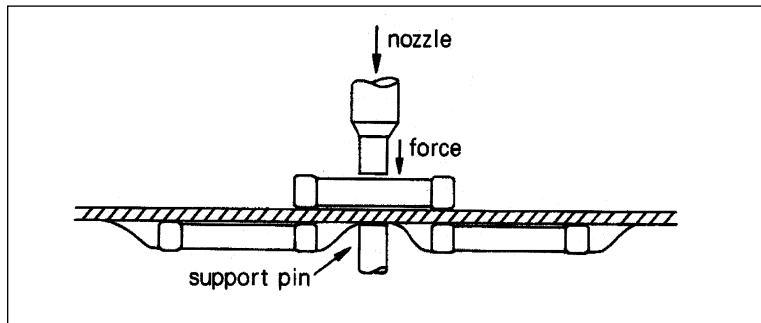
4. Mounting

4-1. Mounting Head Pressure

Excessive pressure will cause chip capacitors to crack. The pressure between nozzle and chip capacitor will be 300g maximum during mounting.

4-2. Bending Stress

Bending of printed circuit board by mounting head when double-sided circuit boards are used, chip capacitors first are mounted and soldered onto one side of the board. When the capacitors are mounted onto the other side, it is important to support the board as shown in the illustration . If the circuit board is not supported, it may bend, causing the already installed capacitors to crack.



5. Flux

Although highly activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitors. To avoid such degradation, it is recommended that a mildly activated rosin flux (less than 0.2% chlorine) be used.

6. Soldering

Since a multilayer chip ceramic capacitor comes into direct contact with melted solder during soldering, it is exposed to potentially damaging mechanical stress caused by the sudden temperature change. The capacitor may also be subject to silver migration, and to contamination by the flux. Because of these factors, soldering technique is critical.

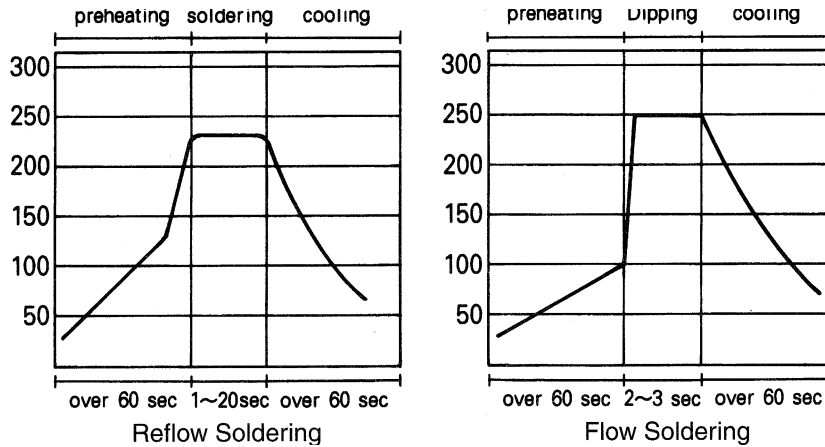
6-1. Soldering Methods

Method	Classification	
Reflow Soldering	Mass reflow	<ul style="list-style-type: none"> • IR/Convection • VPS (Vapor phase)
	Selective reflow	<ul style="list-style-type: none"> • Hot air/gas • Laser
Flow Soldering	Dual Wave	

6-2. Soldering Profile

To avoid the crack problem by sudden temperature change, follow the temperature profile in the adjacent graph.

Multilayer Ceramic Chip Capacitors



6-3. Manual Soldering

Manual Soldering can pose a great risk of creating thermal cracks in chip capacitors. The hot soldering iron tip comes into direct contact with the end terminations, and operator's carelessness may cause the tip of the soldering iron to come into direct contact with the ceramic body of the capacitor. Therefore the soldering iron must be handled carefully, and close attention must be paid to the selection of the soldering iron tip and to temperature control of the tip.

6-4. Amount of Solder

Too much solder		Cracks tend to occur due to large stress
Amount of solder is adequate		Maximum amount of solder Minimum amount of solder
Not enough solder		Weak holding force may cause bad connections or detaching of the capacitor

6-5. Cooling

Natural cooling using air is recommended. If the chips are dipped into solvent for cleaning, the temperature difference (ΔT) must be less than 100°C.

6-6. Cleaning

If rosin flux is used, cleaning usually is unnecessary. When strongly activated flux is used, chlorine in the flux may dissolve into some types of cleaning fluids, thereby affecting the chip capacitors. This means that the cleaning fluid must be carefully selected, and should always be new.

7. Notes for Separating Multiple, Shared PC Boards

A multi-PC board is separated into many individual circuit boards after soldering has been completed. If the board is bent or distorted at the time of separation, cracks may occur in the chip capacitors. Carefully choose a separation method that minimizes the bending of the circuit board.

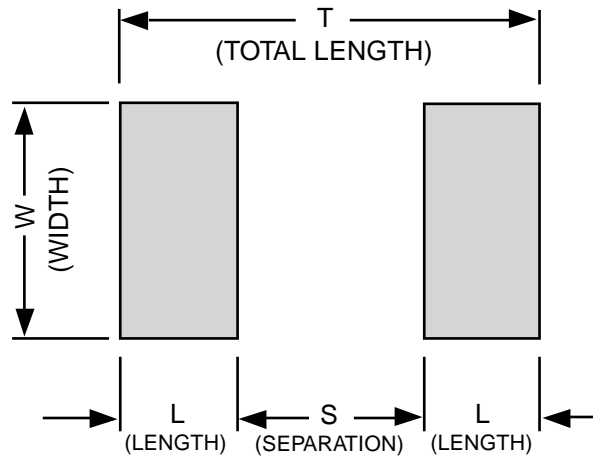
Multilayer Ceramic Chip Capacitors

APPLICATION INFORMATION ON SOLDER PAD DESIGN
FOR SURFACE MOUNT CHIP CAPACITOR

Recommended Pad Dimensions

Chip Size	Dimensions (inches)			
	L	W	S	T
0402*	0.021	0.022	0.017	0.059
0603*	0.035	0.030	0.030	0.100
0805	0.040	0.050	0.040	0.120
0907	0.040	0.070	0.050	0.130
1206	0.040	0.065	0.080	0.160
1210	0.040	0.100	0.080	0.160
1812*	0.050	0.120	0.130	0.230
1825*	0.050	0.250	0.130	0.230
2220	0.050	0.250	0.130	0.230
2225*	0.050	0.250	0.170	0.270
3640*	0.060	0.400	0.300	0.420

*These sizes are recommended for use with IR and vapor phase soldering only.



NOTICE: Specifications are subject to change without notice. Contact your nearest Cal-Chip Sales Office for the latest specifications. All statements, information and data given herein are believed to be accurate and reliable, but are presented without guarantee, warranty, or responsibility of any kind, expressed or implied. Statements or suggestions concerning possible use of our products are made without representation or warranty that any such use is free of patent infringement and are not recommendations to infringe any patent. The user should not assume that all safety measures are indicated or that other measures may not be required. Specifications are typical and may not apply to all applications.

Multilayer Ceramic Chip Capacitors

CHIP MARKING IDENTIFICATION SYSTEM

Marking

Proposed EIA Standard:

Two Position Marking:*

Alpha: 1st position significant figures of capacitance in pF

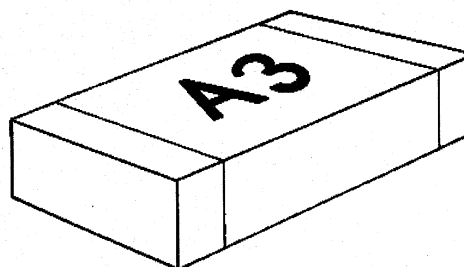
Numerical: 2nd position decimal multiplier of capacitance

NOTE: ¥ 0402, 0603, 0907 available unmarked only.

CAPACITANCE

Letter	0	1	2	3	4	5
A	1.0	10	100	1000	10,000	100,000
B	1.1	11	110	1100	11,000	110,000
C	1.2	12	120	1200	12,000	120,000
D	1.3	13	130	1300	13,000	130,000
E	1.5	15	150	1500	15,000	150,000
F	1.6	16	160	1600	16,000	160,000
G	1.8	18	180	1800	18,000	180,000
H	2.0	20	200	2000	20,000	200,000
J	2.2	22	220	2200	22,000	220,000
K	2.4	24	240	2400	24,000	240,000
L	2.7	27	270	2700	27,000	270,000
M	3.0	30	300	3000	30,000	300,000
N	3.3	33	330	3300	33,000	330,000
P	3.6	36	360	3600	36,000	360,000
Q	3.9	39	390	3900	39,000	390,000
R	4.3	43	430	4300	43,000	430,000
S	4.7	47	470	4700	47,000	470,000
T	5.1	51	510	5100	51,000	510,000
U	5.6	56	560	5600	56,000	560,000
V	6.2	62	620	6200	62,000	620,000
W	6.8	68	680	6800	68,000	680,000
X	7.5	75	750	7500	75,000	750,000
Y	8.2	82	820	8200	82,000	820,000
Z	9.1	91	910	9100	91,000	910,000

Letter	0	1	2	3	4	5
a	2.5					
b	3.5					
d	4.0					
e	4.5					
f	5.0					
m	6.0					
n	7.0					
t	8.0					
y	9.0					
	x1.0	x10	x100	x1000	x10,000	x100,000



**TWO POSITION MARKING
(1000 pF)**